

# BUK9MGP-55PTS

Dual TrenchPLUS logic level FET

Rev. 01 — 14 May 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

### 1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

### 1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

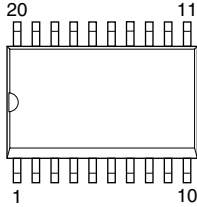
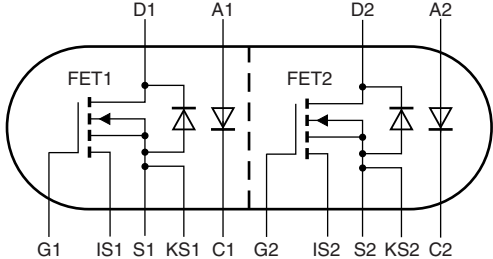
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics, FET1</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 23</a> ; see <a href="#">Figure 25</a>	-	8.6	10	mΩ
$I_D/I_{sense}$	ratio of drain current to sense current	$T_j = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 27</a>	8100	9000	9900	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 250\text{ μA}$ ; $T_j = 25\text{ °C}$	55	-	-	V
<b>Static characteristics, FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 24</a> ; see <a href="#">Figure 26</a>	-	21.3	25	mΩ
$I_D/I_{sense}$	ratio of drain current to sense current	$T_j = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 28</a>	5910	6570	7227	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 250\text{ μA}$ ; $T_j = 25\text{ °C}$	55	-	-	V

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 <p><b>SOT163-1 (SO20)</b></p>	 <p style="text-align: right;">003aaa745</p>
2	IS1	current sense 1		
3	D1	drain 1		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK9MGP-55PTS	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

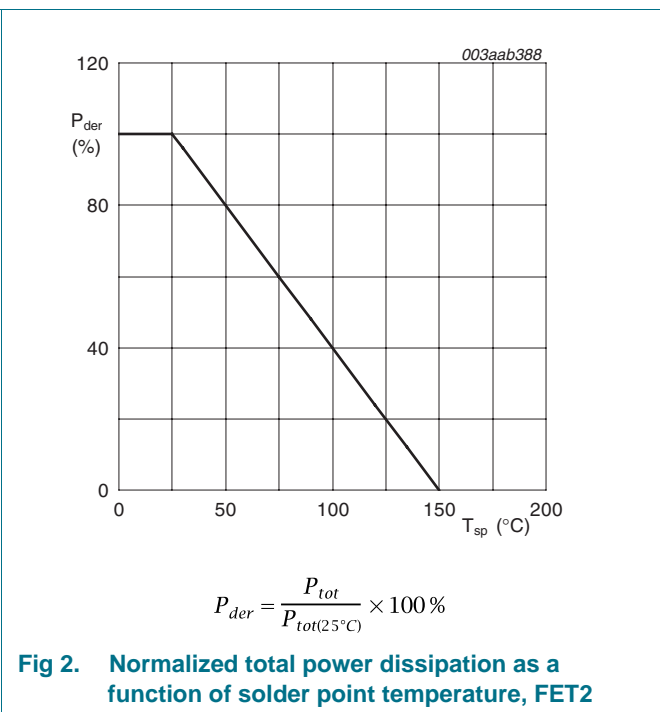
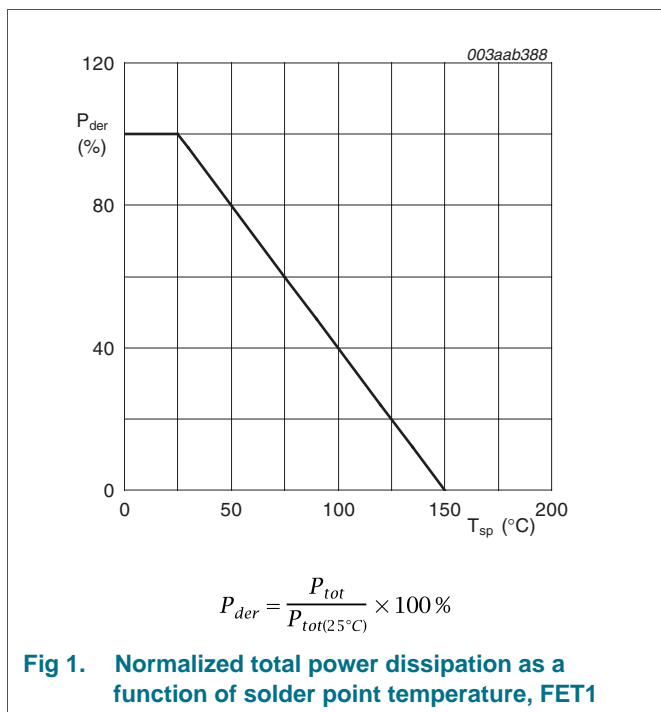
Symbol	Parameter	Conditions	Min	Max	Unit
<b>Limiting values, FET1</b>					
V <sub>DS</sub>	drain-source voltage	25 °C < T <sub>j</sub> < 150 °C	-	55	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ; 25 °C < T <sub>j</sub> < 150 °C	-	55	V
V <sub>GS</sub>	gate-source voltage		-15	15	V
I <sub>D</sub>	drain current	T <sub>sp</sub> = 25 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 3</a> ; see <a href="#">Figure 7</a> ; <a href="#">[1][2]</a>	-	16.9	A
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 3</a> ; <a href="#">[1][2]</a>	-	10.7	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; t <sub>p</sub> ≤ 10 μs; pulsed; see <a href="#">Figure 7</a>	-	349	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see <a href="#">Figure 1</a>	-	5.2	W
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
V <sub>isol(FET-TSD)</sub>	FET to temperature sense diode isolation voltage		-	100	V
<b>Limiting values, FET2</b>					
V <sub>DS</sub>	drain-source voltage	25 °C < T <sub>j</sub> < 150 °C	-	55	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ; 25 °C < T <sub>j</sub> < 150 °C	-	55	V
V <sub>GS</sub>	gate-source voltage		-15	15	V
I <sub>D</sub>	drain current	T <sub>sp</sub> = 25 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 4</a> ; see <a href="#">Figure 8</a> ; <a href="#">[1][2]</a>	-	9.16	A
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 4</a> ; <a href="#">[1][2]</a>	-	5.8	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; t <sub>p</sub> ≤ 10 μs; pulsed; see <a href="#">Figure 8</a>	-	148	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see <a href="#">Figure 2</a>	-	3.9	W
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
V <sub>isol(FET-TSD)</sub>	FET to temperature sense diode isolation voltage		-	100	V
<b>Source-drain diode, FET1</b>					
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C; <a href="#">[1][2]</a>	-	7.3	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>sp</sub> = 25 °C	-	349	A
<b>Source-drain diode, FET2</b>					
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C; <a href="#">[1][2]</a>	-	5.5	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>sp</sub> = 25 °C	-	148	A
<b>Avalanche ruggedness, FET1</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 16.9 A; V <sub>sup</sub> ≤ 55 V; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; see <a href="#">Figure 5</a> ; <a href="#">[3][4]</a> <a href="#">[5]</a>	-	929	mJ
<b>Avalanche ruggedness, FET2</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 9.16 A; V <sub>sup</sub> ≤ 55 V; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; see <a href="#">Figure 6</a> ; <a href="#">[3][4]</a> <a href="#">[5]</a>	-	360	mJ

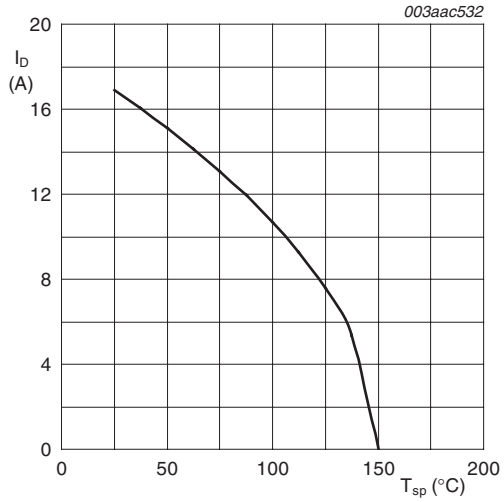
**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Electrostatic discharge, FET1</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted	-	4	kV
		HBM; C = 100 pF; R = 1.5 kΩ; all pins	-	0.15	kV
<b>Electrostatic discharge, FET2</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; pins 8, 11 and 15 to pins 6, 7, 12, 13 and 14 shorted	-	4	kV
		HBM; C = 100 pF; R = 1.5 kΩ; all pins	-	0.15	kV

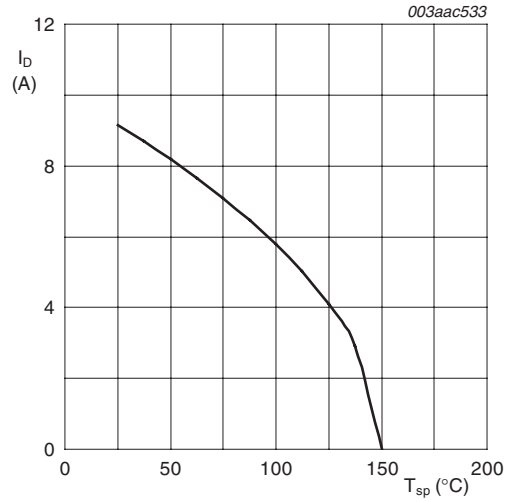
- [1] Single device conducting.
- [2] Current is limited by chip power dissipation rating.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.
- [4] Repetitive rating defined in avalanche rating figure.
- [5] Refer to application note AN10273 for further information.





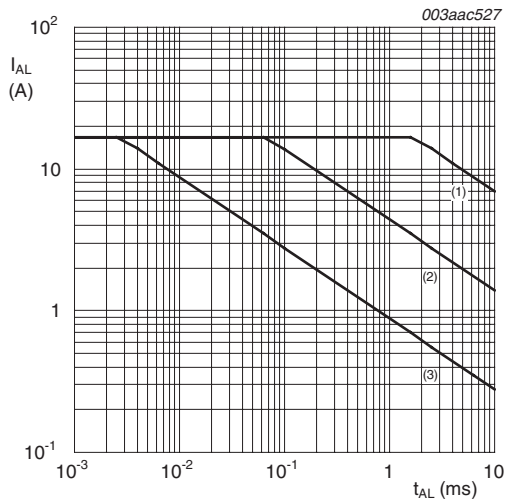
$V_{GS} \geq 5V$

**Fig 3. Continuous drain current as a function of solder point temperature, FET1.**



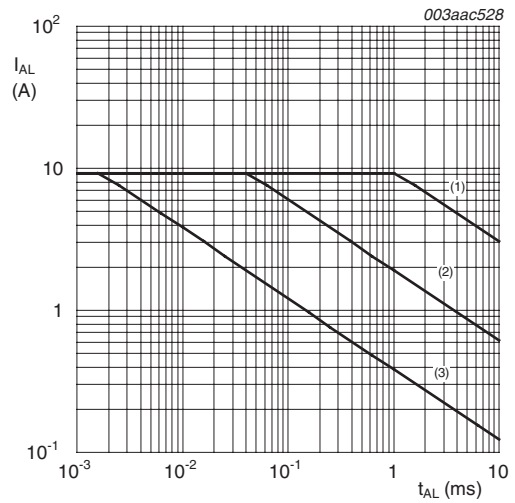
$V_{GS} \geq 5V$

**Fig 4. Continuous drain current as a function of solder point temperature, FET2.**



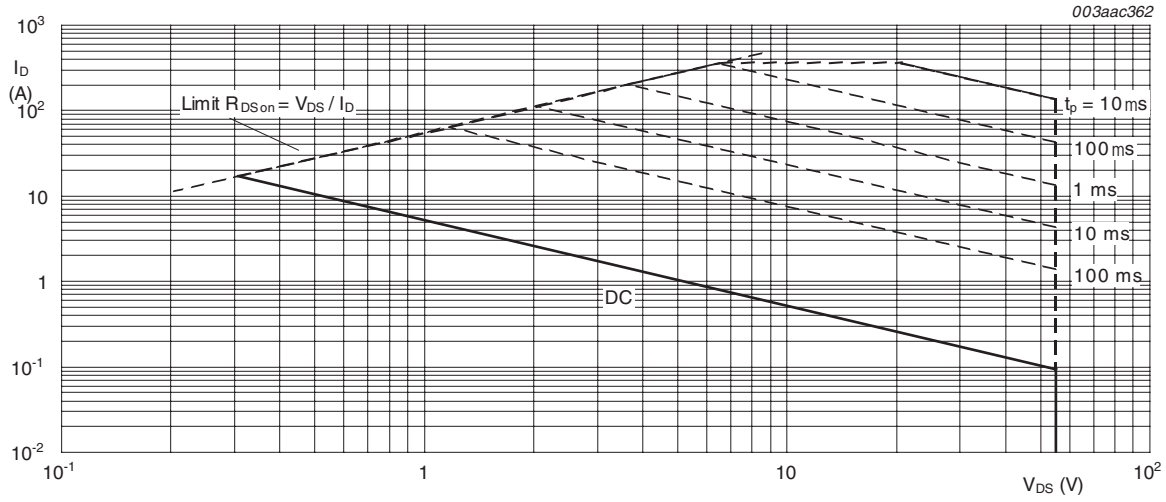
- (1) Single-pulse;  $T_j = 25\text{ °C}$ .
- (2) Single-pulse;  $T_j = 150\text{ °C}$ .
- (3) Repetitive.

**Fig 5. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1**



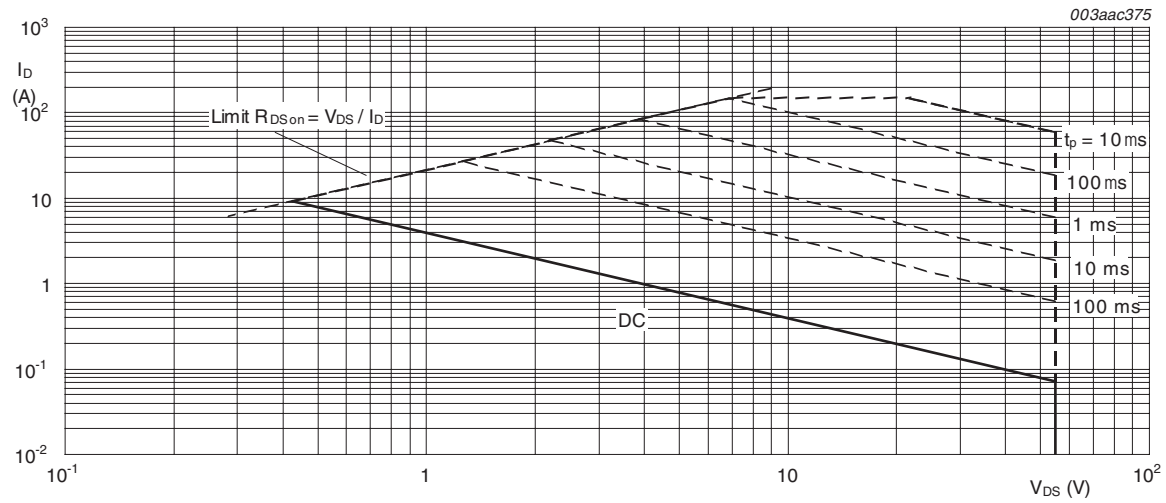
- (1) Single-pulse;  $T_j = 25\text{ °C}$ .
- (2) Single-pulse;  $T_j = 150\text{ °C}$ .
- (3) Repetitive.

**Fig 6. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET2**



$T_{sp} = 25\text{ }^\circ\text{C}; I_{DM}$  is single pulse

**Fig 7. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1.**



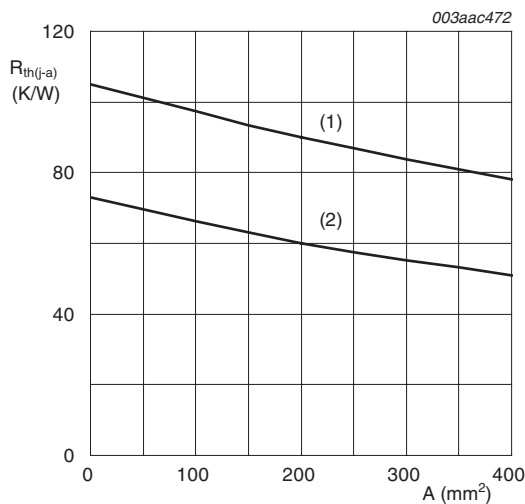
$T_{sp} = 25\text{ }^\circ\text{C}; I_{DM}$  is single pulse

**Fig 8. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET2.**

## 5. Thermal characteristics

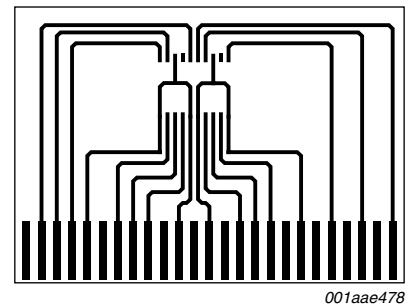
**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	24	K/W
		FET2	-	-	32	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; Both channel conducting; zero heat sink area; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	73	-	K/W
		mounted on printed-circuit board; Both channel conducting; 200 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 9</a> ; see <a href="#">Figure 11</a>	-	60	-	K/W
		mounted on printed-circuit board; Both channel conducting; 400 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 9</a> ; see <a href="#">Figure 12</a>	-	51	-	K/W
		mounted on printed-circuit board; One channel conducting; zero heat sink area; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	105	-	K/W
		mounted on printed-circuit board; One channel conducting; 200 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 9</a> ; see <a href="#">Figure 11</a>	-	90	-	K/W
		mounted on printed-circuit board; One channel conducting; 400 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 9</a> ; see <a href="#">Figure 12</a>	-	78	-	K/W

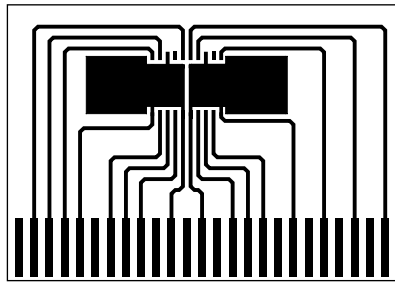


- (1) One channel conducting dissipating 500mW.
  - (2) Both channels conducting each dissipating 500mW.
- Zero air flow

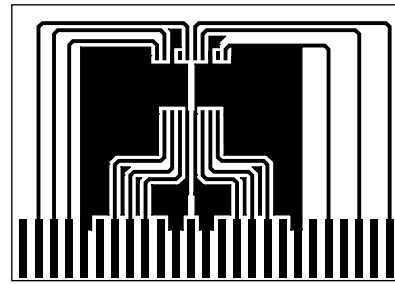
**Fig 9. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area**



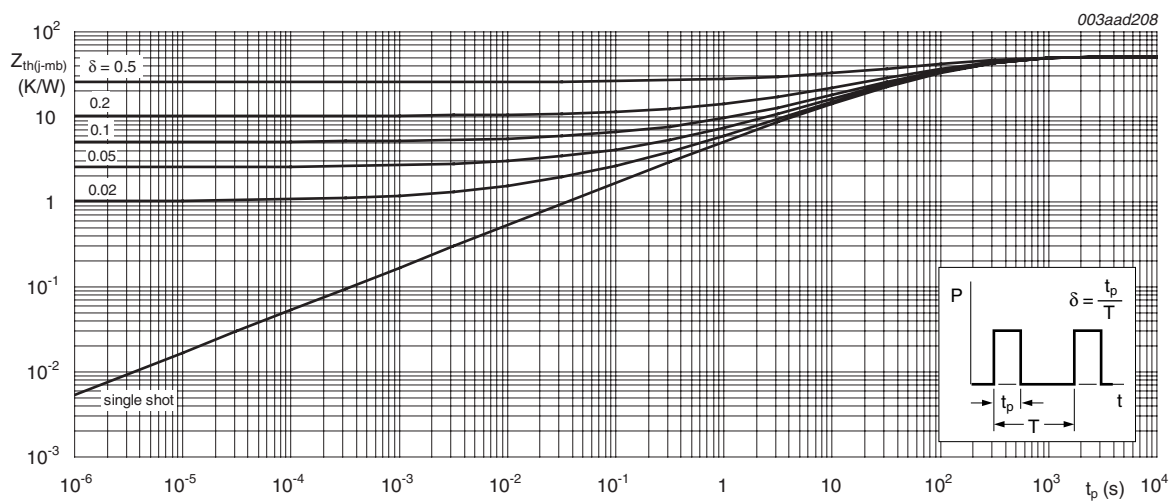
**Fig 10. PCB used for thermal tests; zero heat sink area**



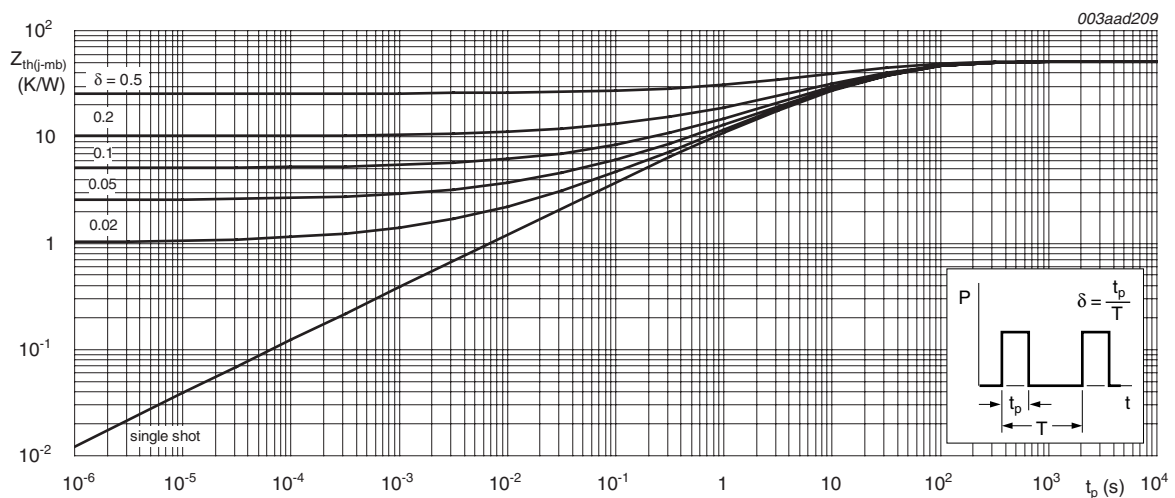
**Fig 11. PCB used for thermal tests; heat sink area 200 mm<sup>2</sup>**



**Fig 12. PCB used for thermal tests; heat sink area 400 mm<sup>2</sup>**



**Fig 13. Transient thermal impedance from junction to ambient as a function of pulse duration, FET1 (PCB used for thermal tests; heat sink area 400mm<sup>2</sup>)**



**Fig 14. Transient thermal impedance from junction to ambient as a function of pulse duration, FET2 (PCB used for thermal tests; heat sink area 400mm<sup>2</sup>)**



## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics, FET1</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 21</a> ; see <a href="#">Figure 22</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 21</a> ; see <a href="#">Figure 22</a>	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 21</a> ; see <a href="#">Figure 22</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	3	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	125	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	300	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 23</a> ; see <a href="#">Figure 25</a>	-	8.6	10	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 25</a> ; see <a href="#">Figure 23</a>	-	-	18	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 23</a> ; see <a href="#">Figure 25</a>	-	9.4	11.1	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 23</a> ; see <a href="#">Figure 25</a>	-	8.1	9	m $\Omega$
$I_D/I_{sense}$	ratio of drain current to sense current	$T_j = 25 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}$ ; see <a href="#">Figure 27</a>	8100	9000	9900	A/A
$S_F(TSD)$	temperature sense diode temperature coefficient	$I_F = 250 \mu\text{A}; 25 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 29</a>	-5.4	-5.7	-6	mV/K
$V_F(TSD)$	temperature sense diode forward voltage	$I_F = 250 \mu\text{A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 29</a>	2.855	2.9	2.945	V
<b>Static characteristics, FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 21</a> ; see <a href="#">Figure 22</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 21</a> ; see <a href="#">Figure 22</a>	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 21</a> ; see <a href="#">Figure 22</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	3	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	125	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	300	nA

**Table 6. Characteristics ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 24</a> ; see <a href="#">Figure 26</a>	-	21.3	25	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 150 °C; see <a href="#">Figure 24</a> ; see <a href="#">Figure 26</a>	-	-	46.8	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 24</a> ; see <a href="#">Figure 26</a>	-	23.7	27.9	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 24</a> ; see <a href="#">Figure 26</a>	-	20.3	22.6	mΩ
I <sub>D</sub> /I <sub>sense</sub>	ratio of drain current to sense current	T <sub>j</sub> = 25 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 28</a>	5910	6570	7227	A/A
S <sub>F(TSD)</sub>	temperature sense diode temperature coefficient	I <sub>F</sub> = 250 μA; 25 °C < T <sub>j</sub> < 150 °C; see <a href="#">Figure 29</a>	-5.4	-5.7	-6	mV/K
V <sub>F(TSD)</sub>	temperature sense diode forward voltage	I <sub>F</sub> = 250 μA; T <sub>j</sub> = 25 °C; see <a href="#">Figure 29</a>	2.855	2.9	2.945	V

**Dynamic characteristics, FET1**

Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 44 V; V <sub>GS</sub> = 5 V; see <a href="#">Figure 30</a>	-	54	-	nC
Q <sub>GS</sub>	gate-source charge		-	9.4	-	nC
Q <sub>GD</sub>	gate-drain charge		-	21.5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 32</a>	-	3884	5178	pF
C <sub>oss</sub>	output capacitance		-	540	648	pF
C <sub>rss</sub>	reverse transfer capacitance		-	247	338	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 3 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 10 Ω	-	41	-	ns
t <sub>r</sub>	rise time		-	94	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	184	-	ns
t <sub>f</sub>	fall time		-	98	-	ns
L <sub>D</sub>	internal drain inductance	From pin to centre of die	-	0.85	-	nH
L <sub>S</sub>	internal source inductance	From source lead to source bonding pad	-	1.9	-	nH

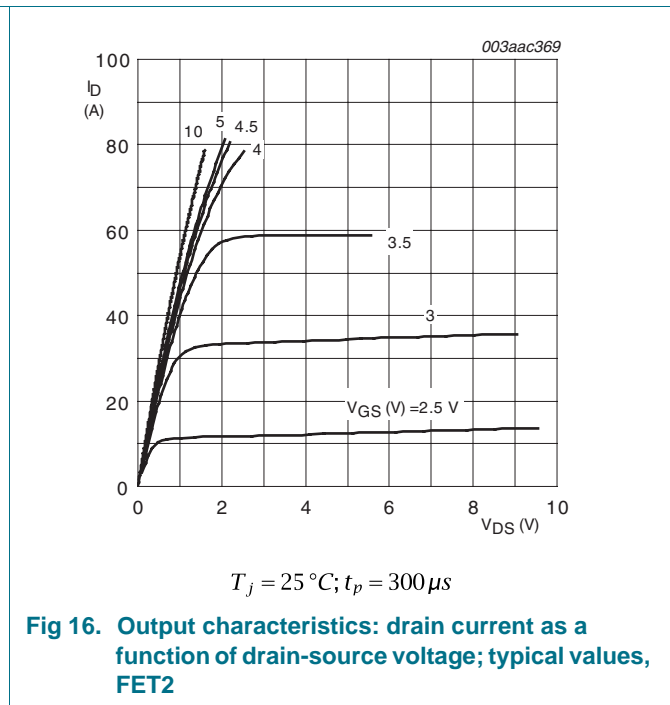
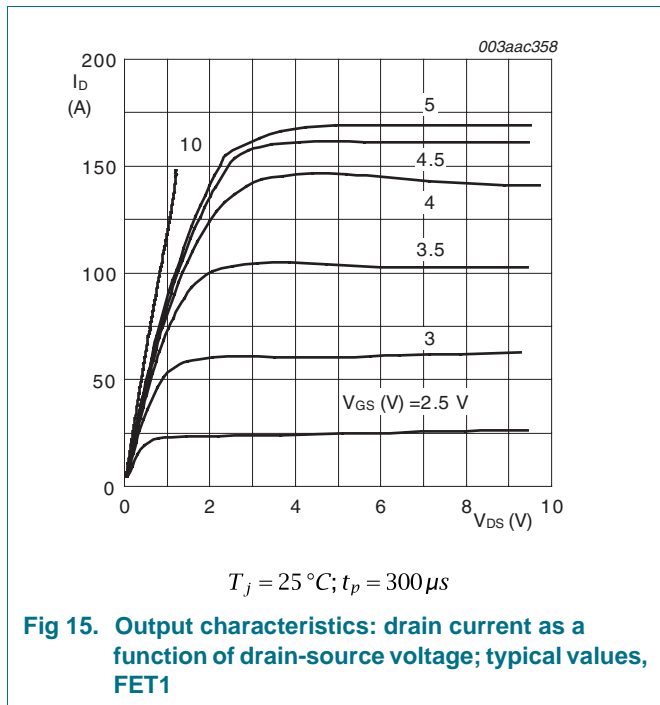
**Dynamic characteristics, FET2**

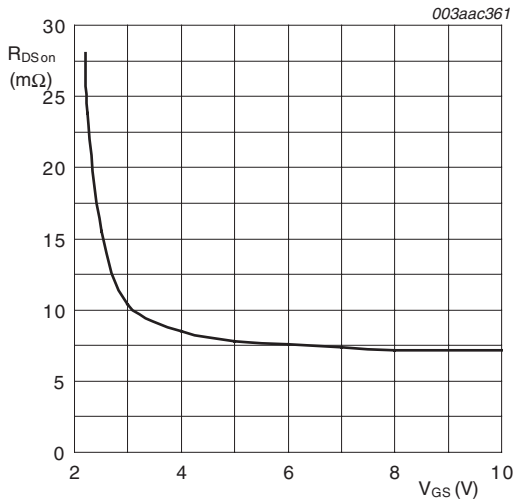
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 44 V; V <sub>GS</sub> = 0 V; see <a href="#">Figure 31</a>	-	23	-	nC
Q <sub>GS</sub>	gate-source charge		-	3.4	-	nC
Q <sub>GD</sub>	gate-drain charge		-	9	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 33</a>	-	1736	2315	pF
C <sub>oss</sub>	output capacitance		-	244	293	pF
C <sub>rss</sub>	reverse transfer capacitance		-	119	163	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 6 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 10 Ω	-	29	-	ns
t <sub>r</sub>	rise time		-	44	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	91	-	ns
t <sub>f</sub>	fall time		-	46	-	ns

**Table 6. Characteristics ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$L_D$	internal drain inductance	From pin to centre of die	-	0.85	-	nH
$L_S$	internal source inductance	From source lead to source bonding pad	-	2	-	nH
<b>Source-drain diode, FET1</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 34</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = -10\text{ V}$ ; <a href="#">[1]</a>	-	66.4	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}$ ;	-	126	-	nC
<b>Source-drain diode, FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 35</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = -10\text{ V}$ ;	-	44	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}$	-	69	-	nC

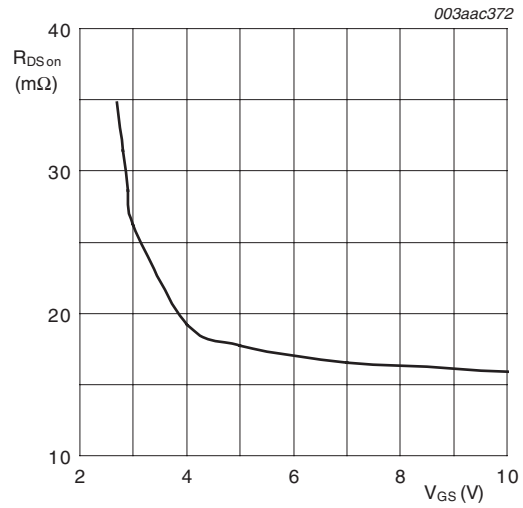
[1] xsa





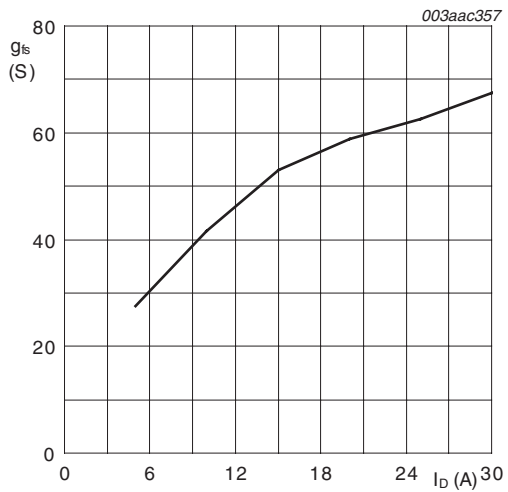
$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$

**Fig 17. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1**



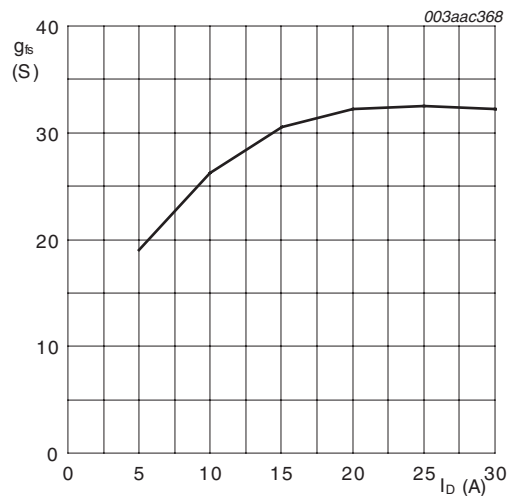
$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$

**Fig 18. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET2**



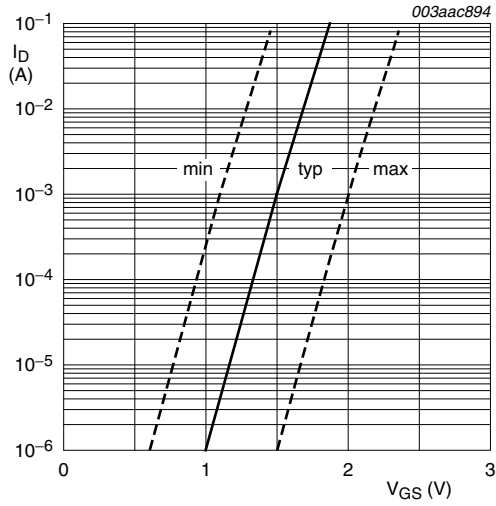
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

**Fig 19. Forward transconductance as a function of drain current; typical values, FET1**



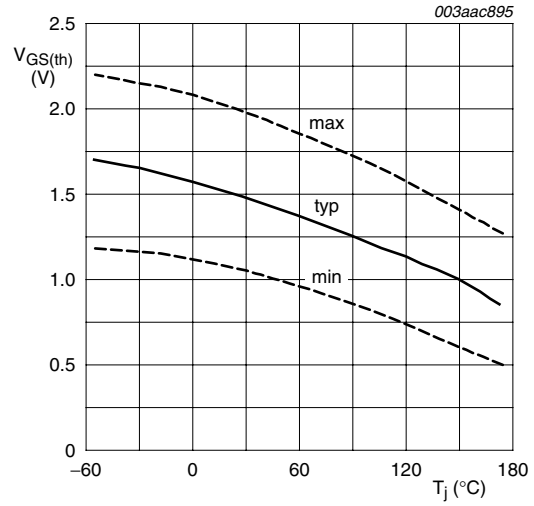
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

**Fig 20. Forward transconductance as a function of drain current; typical values, FET2**



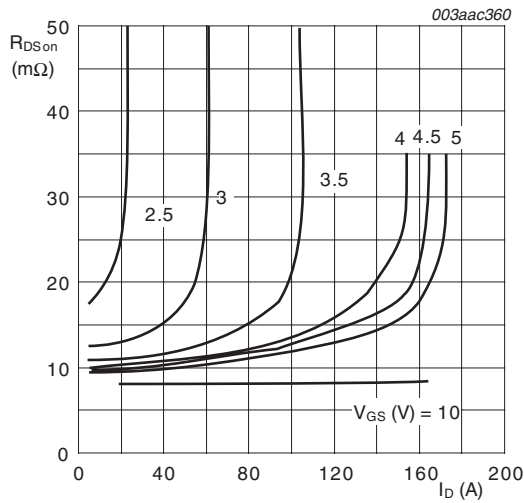
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

**Fig 21. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2**



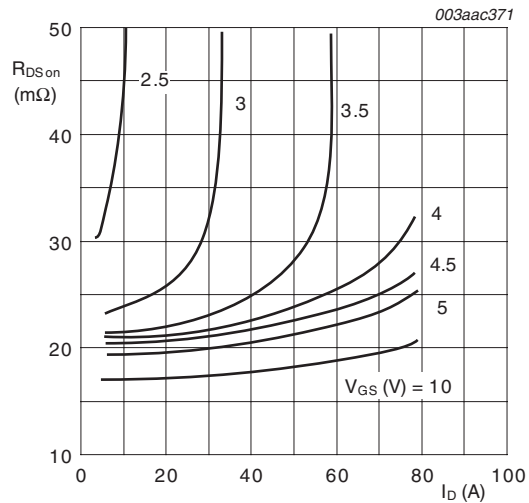
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

**Fig 22. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2**



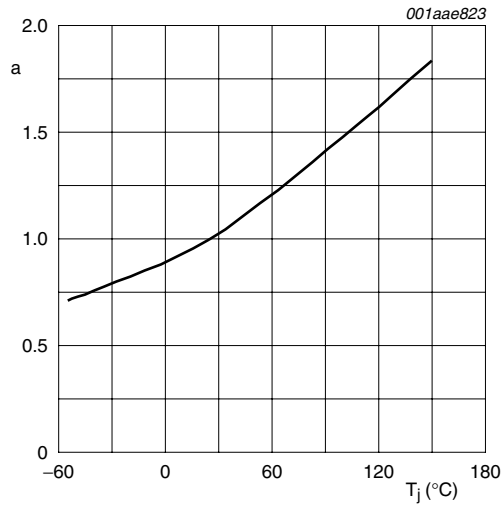
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig 23. Drain-source on-state resistance as a function of drain current; typical values, FET1**



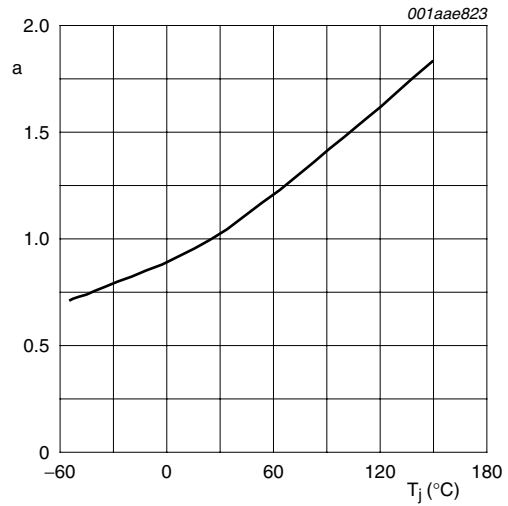
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig 24. Drain-source on-state resistance as a function of drain current; typical values, FET2**



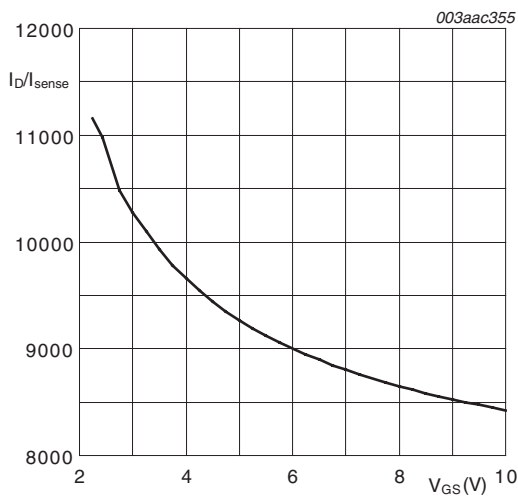
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 25. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1**



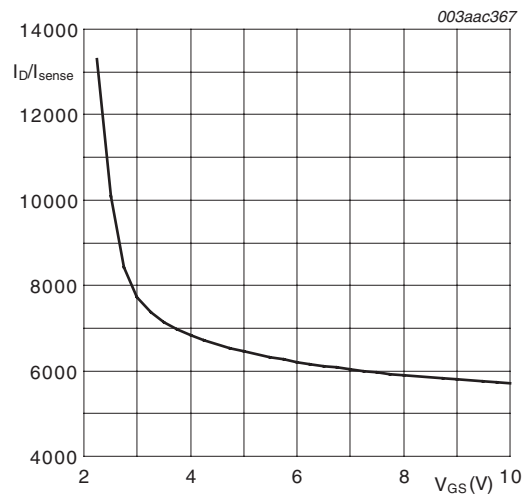
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 26. Normalized drain-source on-state resistance factor as a function of junction temperature, FET2**



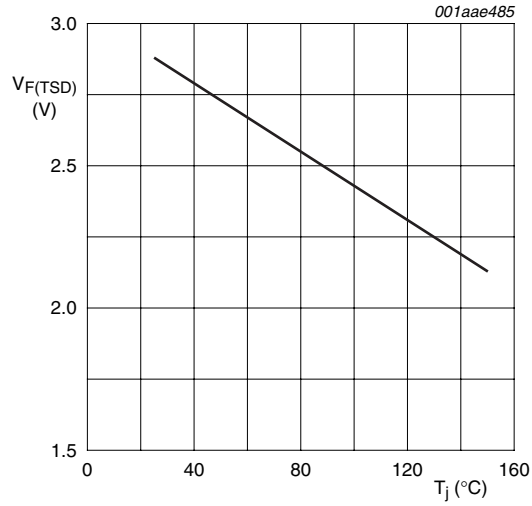
$$T_j = 25^{\circ}C; I_D = 5A$$

**Fig 27. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1**



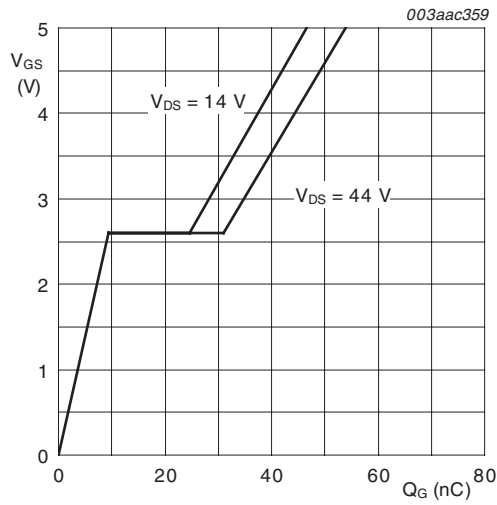
$$T_j = 25^{\circ}C; I_D = 5A$$

**Fig 28. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET2**



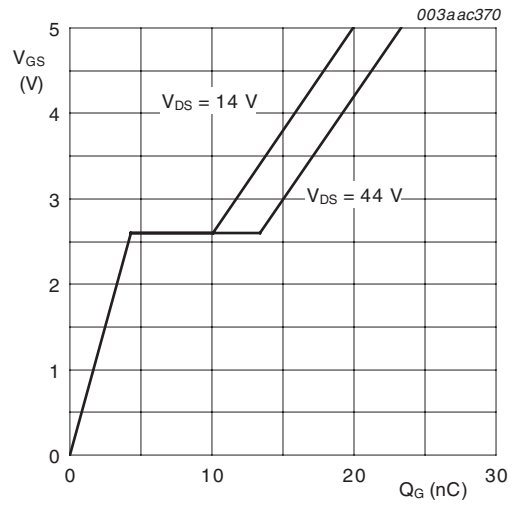
$I_F = 250 \mu A$

**Fig 29. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2**



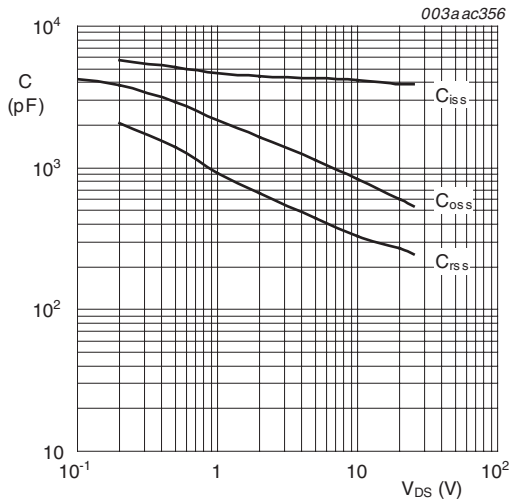
$T_j = 25 \text{ }^\circ\text{C}; I_D = 10 A$

**Fig 30. Gate-source voltage as a function of turn-on gate charge; typical values, FET1**



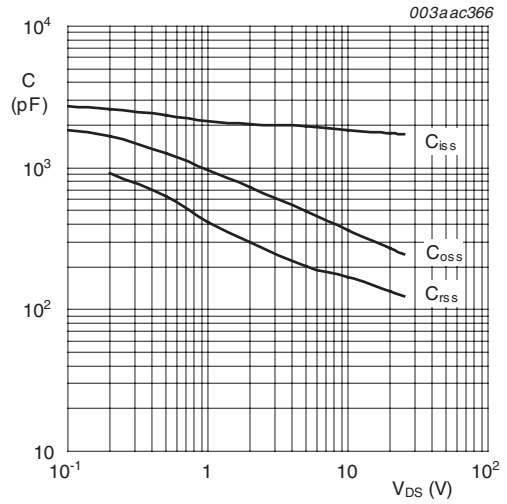
$T_j = 25 \text{ }^\circ\text{C}; I_D = 10 A$

**Fig 31. Gate-source voltage as a function of turn-on gate charge; typical values, FET2**



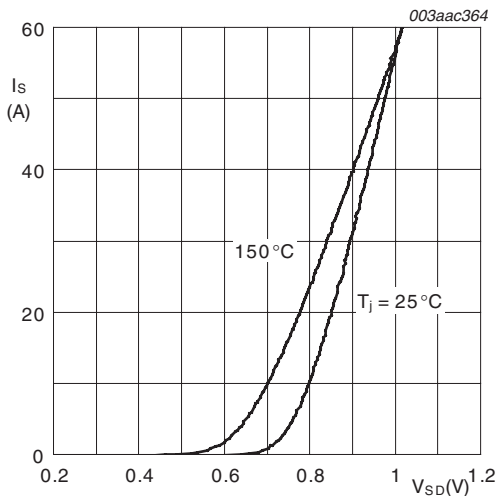
$V_{GS} = 0V; f = 1MHz$

**Fig 32. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1**



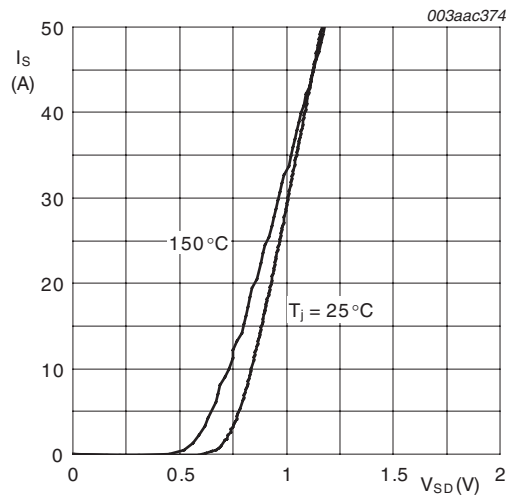
$V_{GS} = 0V; f = 1MHz$

**Fig 33. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET2**



$V_{GS} = 0V$

**Fig 34. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1**



$V_{GS} = 0V$

**Fig 35. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET2**



**7. Package outline**

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

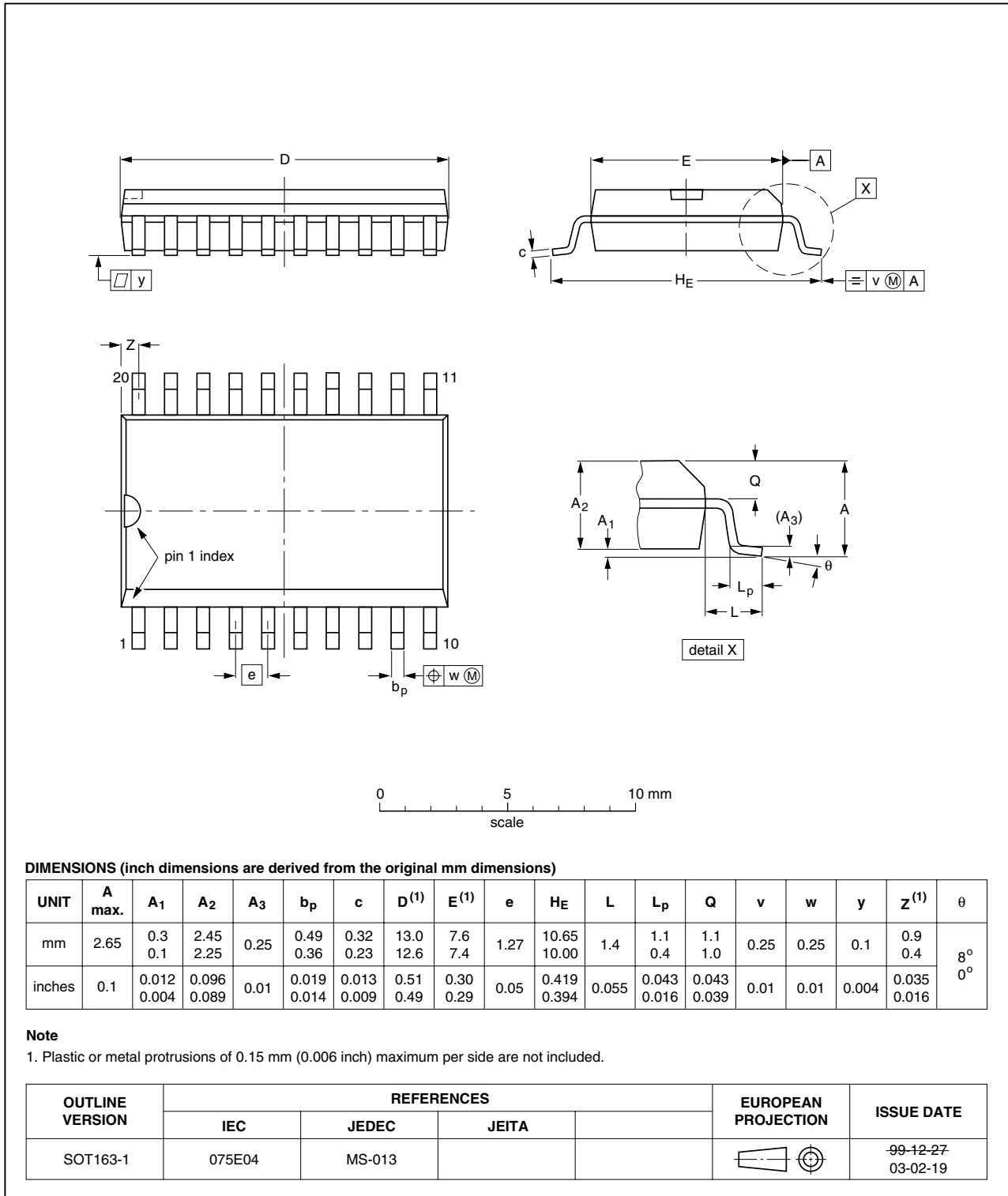


Fig 36. Package outline SOT163-1

## 8. Revision history

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Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MGP-55PTS_1	20090514	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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